# AceProx

# 680-52 REV2 Proximity Reader Module

# Data Sheet

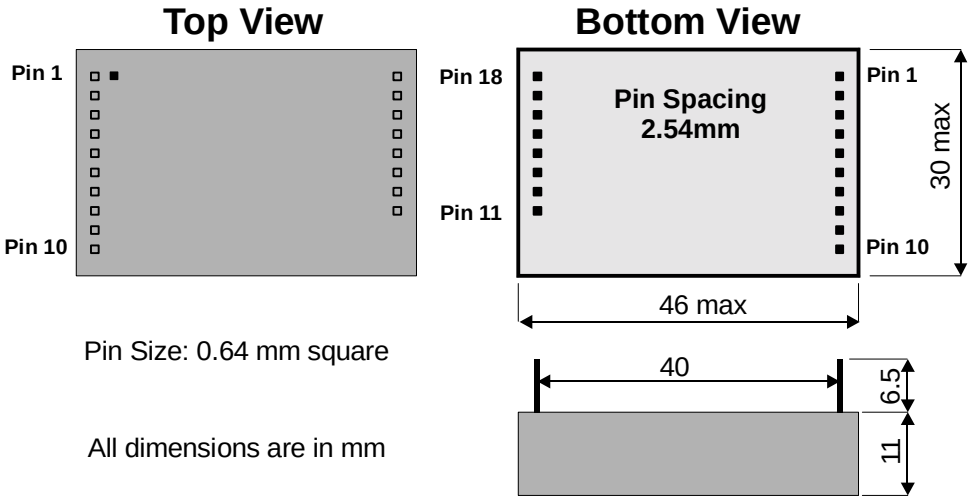
## Overview

The 680-52 proximity reader module is a fully-encapsulated device that will read the code from an RFID transponder and output the code in one of many user selectable formats. The module contains all detection circuitry required to implement a proximity reader including an internal coil antenna. A larger external reader coil may be connected if greater reading range is required.

## Specifications

- Power requirements - either regulated 5V dc or unregulated 7 - 12V dc. Current consumption is 50 mA when idle, 75mA peak while outputing a code which lasts between 20 and 50 ms, and 15mA while in INHIBIT mode.
- RF Frequency: 125 kHz.
- 40 bit read only transponders supported: EM4001 family, TEMIC e5550 and equivalent devices.
- Output formats supported: Wiegand (42-bit, 34-bit, and 26-bit), Mag Stripe emulation, Clock/Data, RS232 (9600,n,8,1) TTL levels, Crosspoint card decoding.
- Continuous (while tag in the field) or single transmission.
- Typical reading range of internal antenna: tag with 20mm coil - 50mm, ISO card with 50mm coil - 90mm, half shell card with 65mm x 40 mm coil - 110mm.
- Piezzo sounder control.
- Operating temperature range: -10ºC - +50ºC.
- Weight: <30 grams.

## Pinout Description & Dimensions



| Pin # | Pin name | Function |
|---|---|---|
| 1 | DETECT | Pulses low when an RFID tag is detected. It stays low while the module output is active. |
| 2 | CLOCK/DATA0 | Outputs RFID tag code in selected format. |
| 3 | DATA/DATA1 | Outputs RFID tag code in selected format. |
| 4 | CONTINUOUS | Connect to 0V for continuous transmission mode. Connect to +5V for single transmission mode. Do not leave disconnected. |
| 5 | INVERT | Connect this pin to 0V to invert output on pins 1,2,3. |
| 6 | SELECT1 | The user can connect to 0V or leave disconnected to select different output formats. |
| 7 | SELECT2 | |
| 8 | SELECT3 | |
| 9 | SELECT4 | |
| 10 | Reserved | Leave disconnected. |
| 11 | COILA | External coil connection. |
| 12 | COILLINK | Link pins 11 and 12 to select internal coil. |
| 13 | COILB | External coil connection. |
| 14 | RAW DATA | Outputs the raw data stream detected from the tag. |
| 15 | BEEPER | Open collector output for connection to an external beeper. |
| 16 | +5V | Direct connection to the module's 5V rail. |
| 17 | +7-12V | Connect +7V - +12V from power supply. |
| 18 | 0V | Connect 0V from power supply. |

## Output Mode Selection

The module has four mode selection pins (SELECT1 ... SELECT4). These pins are internally pulled high in the module. To select the different modes the SELECT pins may be tied to 0V (indicated as 0) or left unconnected (indicated as 1) according to the following table:

| SELECT4 | SELECT3 | SELECT2 | SELECT1 | Output Mode |
|---|---|---|---|---|
| 0 | 0 | 0 | 0 | Inhibit - turn off coil |
| 0 | 0 | 0 | 1 | RS232 - 24 bit |
| 0 | 0 | 1 | 0 | RS232 - 32 bit |
| 0 | 0 | 1 | 1 | RS232 - 40 bit |
| 0 | 1 | 0 | 0 | *Unused* |
| 0 | 1 | 0 | 1 | *Unused* |
| 0 | 1 | 1 | 0 | Fast Mag Stripe - 32 bit |
| 0 | 1 | 1 | 1 | Crosspoint |
| 1 | 0 | 0 | 0 | Fast Mag Stripe - 40 bit |
| 1 | 0 | 0 | 1 | Mag Stripe - 24 bit |
| 1 | 0 | 1 | 0 | Mag Stripe - 32 bit |
| 1 | 0 | 1 | 1 | Mag Stripe - 40 bit |
| 1 | 1 | 0 | 0 | Basic Clock/Data |
| 1 | 1 | 0 | 1 | Wiegand - 26 bit |
| 1 | 1 | 1 | 0 | Wiegand - 34 bit |
| 1 | 1 | 1 | 1 | Wiegand - 42 bit |

## Power Connections

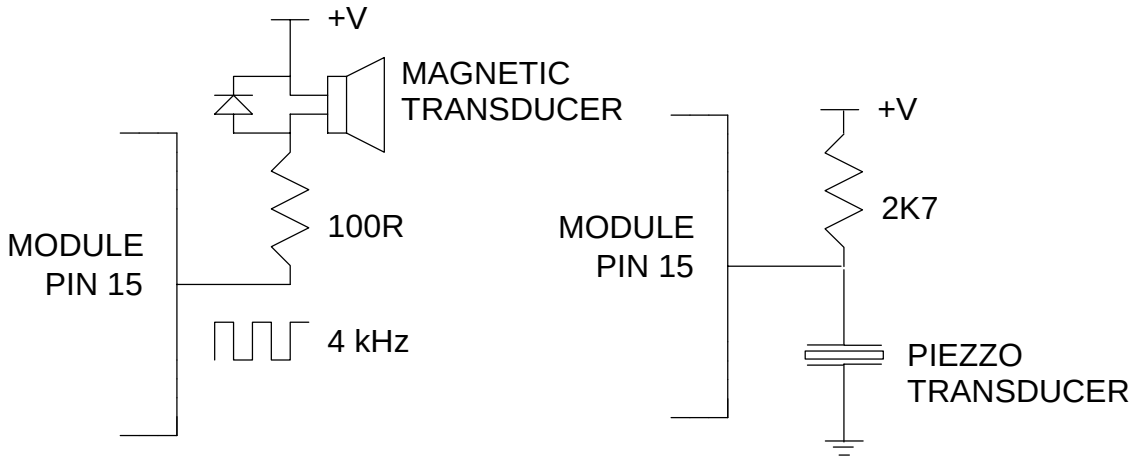
Power can be supplied to the module in two ways:

1. Connect 7-12V across pin 17 (+V) and pin 18 (0V). The module has an internal voltage regulator providing +5V to the circuit. The input to this regulator (pin 17) requires 7-12V d.c. **Do not exceed +12V on this pin.** Note that pin 16 (+5V) is the output of the internal voltage regulator. This is not intended to supply +5V to any external circuitry.
2. Alternatively the internal voltage regulator may be bypassed. Regulated +5V may be connected across pin 16 (+5V) and pin 18 (0V). **Do not exceed +5.5V on this pin.**

**Note:** The supply voltage does not affect the reading distance.

## External Beeper Connection

The module pin 15 (BEEPER) is an open collector output. It outputs a frequency of 4 kHz for 60 ms when a tag is read. Two typical circuits are:




## Coil Connection

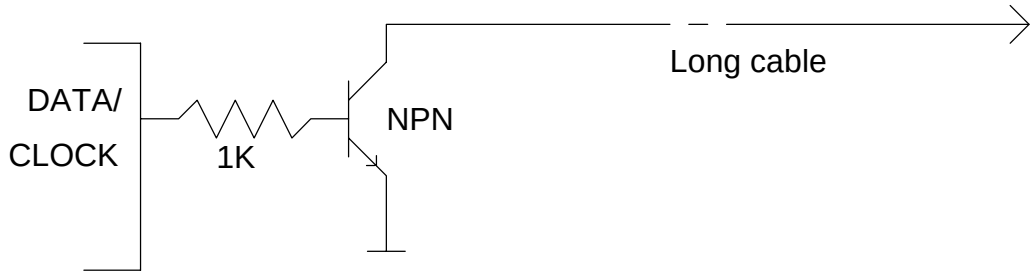
The module has an internal coil which may be suitable for many applications. The internal coil is selected by connecting pin 11 (COILA) to pin 12 (COILLINK).

If an **external** coil is required to obtain a greater reading range, a coil of 486 µH-508µH must be connected between pin 11 (COILA) and pin 13 (COILB). Pin 12 (COILLINK) must be left unconnected. No other external components are required.

## INVERT pin

The polarity of DETECT (pin1), CLOCK/DATA0 (pin2) and DATA/DATA1 (pin3) may be inverted by connecting INVERT (pin 5) to 0V.

In most modes the idle level of the signal pins 1,2 and 3 is high. This is acceptable when connecting the module directly to the receiving equipment over a short cable (<15m). However when a long cable exists between module and receiving equipment it is desirable to include an open collector transistor stage between the module and the long cable as shown below:




To ensure that the idle state of the transistor is off, the idle level from the module signal pins must be low. To achieve this connect INVERT to 0V.
Note that the INVERT pin has no affect on the RS232 modes.

## RS232 (TTL) output modes

The RS232 output from the module is on pin 3 (DATA). This output is suitable to connect directly to the UART of a microprocessor. The idle level is high. The baud rate is 9600. Data format is 8 bits, no parity, and 1 stop bit.

To achieve true RS232 levels the module output should be connected to a level shifter IC (e.g. MAX232).

The tag code is output in the following structure:

| STX (02h) | DATA (ASCII) | CR (0Dh) | LF (0Ah) | ETX (03h) |
|---|---|---|---|---|

The DATA bytes vary according to the number of bits being output:

### 40 bit mode

DATA = 10 ASCII characters representing the 40 bit hexadecimal code of the tag e.g. '0410B2F12A' (30 34 31 30 42 32 46 31 32 41 hex)

### 32 bit mode

DATA = 10 ASCII characters representing the least significant 32 bits of the tag converted to a decimal number e.g. '0280162602' (30 32 38 30 31 36 32 36 30 32 hex)

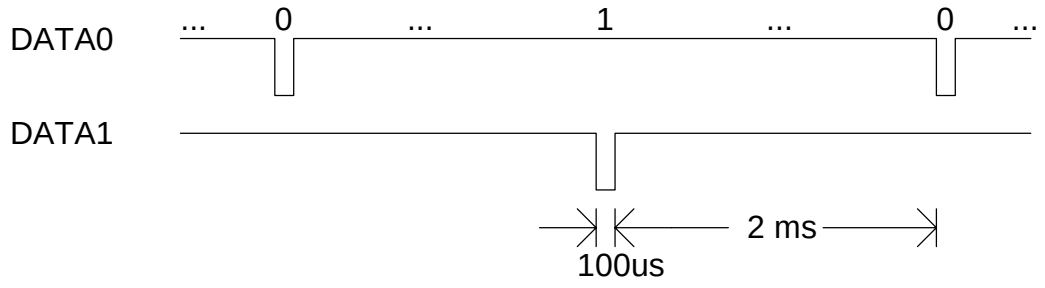
### 24 bit mode

DATA = 8 ASCII characters representing the least significant 24 bits of the tag converted to a decimal number e.g. '11727146' (31 31 37 32 37 31 34 36 hex)

## Wiegand Output Modes

In this mode the tag code is pulsed out on DATA0 (pin 2) and DATA1 (pin 3). Both are normally high. When a tag is presented to the reader 26/34/42 bits are transmitted in the following way:

A binary 1 is represented by a 100 us pulse low on DATA1. A binary 0 is represented by a 100 us pulse low on DATA0. There is a 2 ms inter bit delay.




### 42 bit mode

42 pulses are transmitted:

- The first bit is the even parity of tag bits 1-20.
- All 40 bits of the tag code (MSB first).
- The last bit is the odd parity of tag bits 21-40.

## 34 bit mode

34 pulses are transmitted:

- The first bit is the even parity of tag bits 9-24.
- The least significant 32 bits of the tag code (MSB first).
- The last bit is the odd parity of tag bits 25-40.

## 26 bit mode

26 pulses are transmitted:

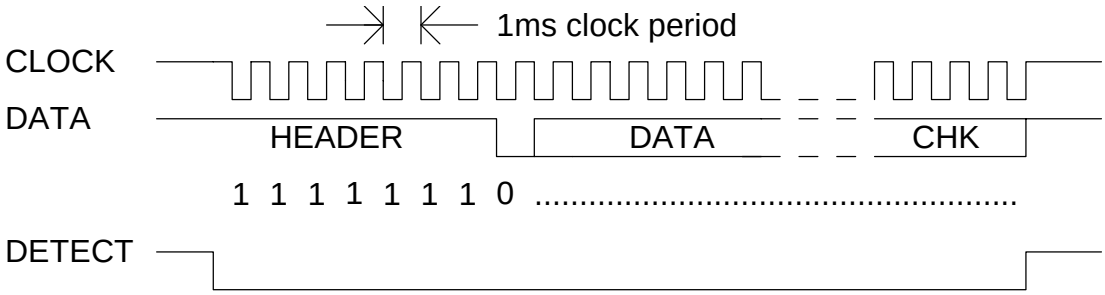
- The first bit is the even parity of tag bits 17-28.
- The least significant 24 bits of the tag code (MSB first).
- The last bit is the odd parity of tag bits 29-40.

## Clock/Data Mode

In this mode all 40 bits of the tag are clocked out with an eight bit header and an eight bit checksum.

| Header (11111110) | Data (40 bits) | Checksum |
|---|---|---|

The header is hex FE. The data consists of all 40 tag bits sent MSB first. The checksum is a byte addition of the 5 bytes of tag data e.g tag 0410B2F12A has a checksum of 04+10+B2+F1+2A=E1.




Data is set up on the falling edge of the clock and is stable on the rising edge of the clock.

## Mag Stripe Modes

In this mode the decimal tag number is clocked out on CLOCK and DATA pins at 100 characters per second. The format is standard as found on Track 2 of a magnetic card:

| 10 leading 0's | SS | DATA | ES | LRC | 5 trailing 0's |
|---|---|---|---|---|---|

SS = start sentinel (B hex).
ES = end sentinel (F hex).
LRC = longitudinal redundancy check.

DATA varies according to the number of bits selected:

## 40 bit mode

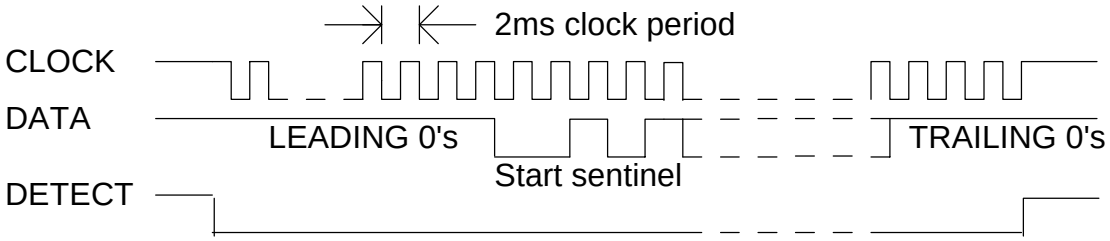
DATA = 13 decimal digits with leading zeros. The most significant decimal digit is transmitted first.

## 32 bit mode

DATA = 10 decimal digits with leading zeros. The most significant decimal digit is transmitted first.

## 24 bit mode

DATA = 8 decimal digits with leading zeros. The most significant decimal digit is transmitted first.




Each character is 5 bits long. The first four bits are the hex digit (0-F) least significant bit first. The fifth bit is an odd parity bit. A 0 is represented by a high level on the DATA pin and a 1 is represented by a low level on the DATA pin. Data is set up on the falling edge of the clock and is stable on the rising edge of the clock. The DETECT pin goes low for the duration of the transmission simulating the CARD DETECT from a mag card reader.

## Fast 40 bit mode

This mode differs from the standard 40bit magstripe mode in the following ways:

- DATA=14 decimal digits with leading zeros.
- The clock period is 200us.
- 10 trailing 0's

All other aspects of this format are the same as the other magstripe formats.

## Fast 32 bit mode

This mode differs from the standard 32bit magstripe mode in the following ways:

- The clock period is 200us.
- 10 trailing 0's

All other aspects of this format are the same as the other magstripe formats.

## Crosspoint mode

In this mode the module assumes the card is encoded as per the Crosspoint bit scrambling algorithm. The unscrambled decimal tag number is clocked out on CLOCK and DATA pins at 1000 characters per second. The clock period is 200us. The format is standard as found on Track 2 of a magnetic card:

| 10 leading 0's | SS | DATA | ES | LRC | 10 trailing 0's |
|---|---|---|---|---|---|

SS = start sentinel (B hex).
ES = end sentinel (F hex).
LRC = longitudinal redundancy check.

DATA = 9 decimal digits with leading zeros. The most significant decimal digit is transmitted first.